Department of BE(E)

Course Details

→ Course Title:- Electronic circuit Design
→ Module :- 4th
→ Instructor :- Engr Mujtaba Ihsan
→ Total Marks :- 30

Student Details

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Q:- 2 A certain operational amplifier has a common mode gain of 0.6 and an open loop differential voltage gain of 400,000, Evaluate the CMRR & express it in decibels.

Sol:- Given data:

→ Aol = open loop differential voltage gain = 400,000

→ ACm = Common mode gain = 0.6

Required:

→ CMRR = ?

Solution:

By formula AS

$$CMRR = \frac{Aol}{ACm}$$

$$= \frac{400,000}{0.6}$$

$$= 666666.6667$$

→ CMRR in decibels:
By formula

→ $CMRR = 20 \log (A_{OL}/A_{CM})$

$= 20 \log (666666.6667)$

$= 116.48$ dB.

* * *

Q:-3
(a) Explain the concept behind negative feedback in operational amplifiers.

Solution. As the open loop DC gain of an operational amplifier is extremely high we can therefore afford to lose some of this high gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces and effect known commonly as Negative feedback and thus produces a very stable operational Amplifier based system.

→ Negative feed back is the process of "feeding back" a fraction of the output signal back to the input, but to make the feedback negative, we must feed it back to the negative or "inverting input" terminal of the operational amplifier using an external Feedback Resistor called Rf.

This feedback connection between the output and the inverting input terminal forces the differential input voltage toward zero.

→ This effect produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its closed-Loop Gain. Then a closed-loop inverting amplifier uses negative feedback to accurately control the overall gain of the amplifier, but at a cost in the reduction of the amplifier gain.

→ Connecting the output of an operational amplifier to its inverting (–) input is called Negative feedback. This term can be broadly applied to any dynamic system where the output signal is "feed back" to the input somehow so as to reach a point of equilibrium (balance).

* * *

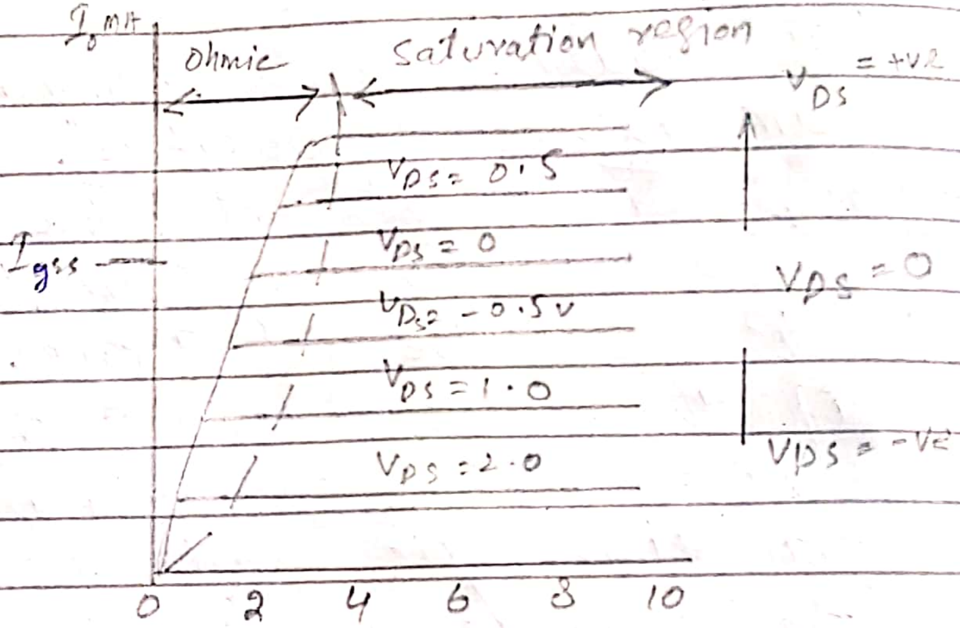
(b) State the following statement as True or False and also give the reason for your answer:
"The output of a summing amplifier is positive".

Ans:- The statement "The output of a summing amplifier is positive" is False because the output of a summing amplifier is Negative.

Reason:-

When the summing point is connected to the inverting input of the operational amplifier the circuit will produce the negative sum of any numbers of input voltages. likewise when the summing point is connected to the non-inverting input of the op-amp. it will produce the positive sum of the input voltage.

Q.1 (a) Explain the drain characteristic curve of D-MOSFET given below:



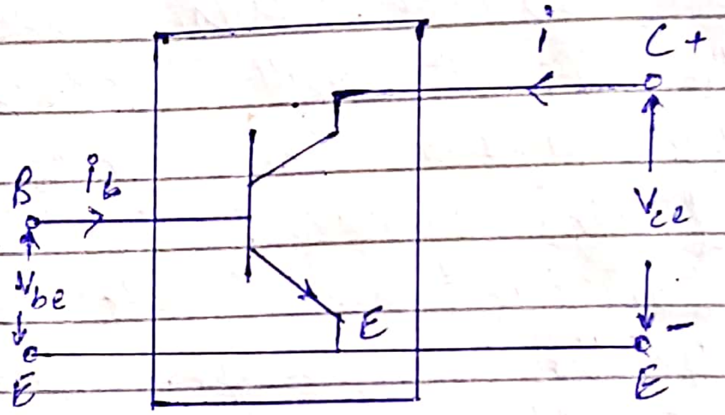
Solution:-

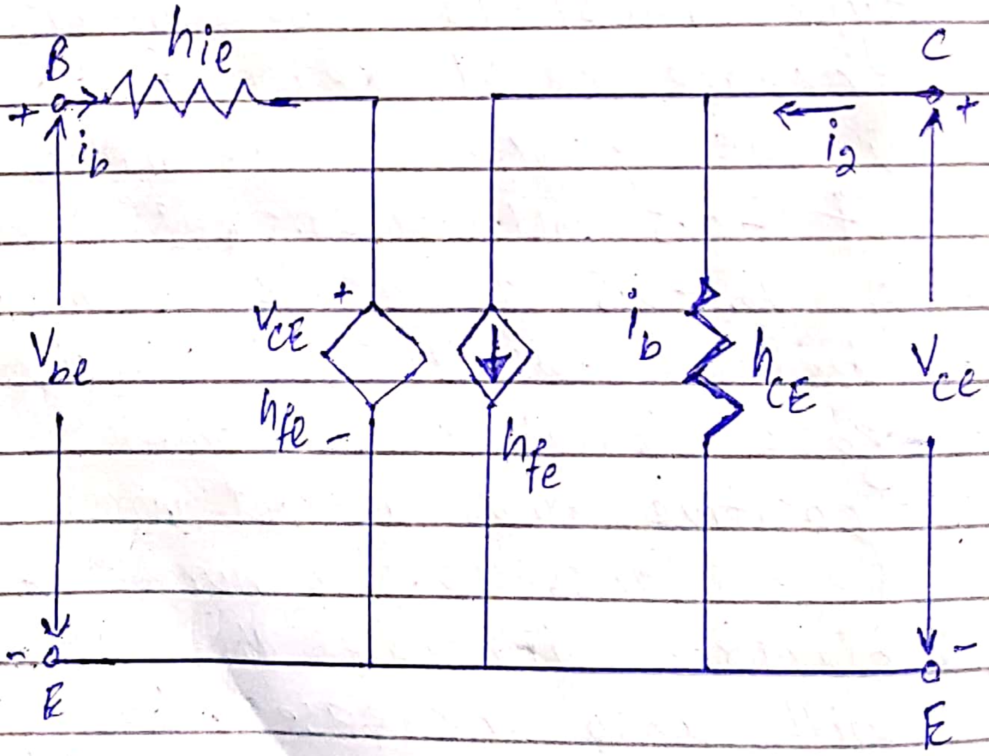
⇒ The channel between drain and source acts as a good conductor with zero Bias voltage at gate terminal. The channel width and drain current increases if the gate voltage is positive and these two (channel width and drain current) decreases if the gate voltage is negative!

⇒ When V_{DS} is zero I_D is also zero this is because there is no potential difference. Hence the potential at drain is same as the potential at source. When we increase V_{ds} the I_D will increase linearly, But after some time the drain current I_d become constant and its because of the pinch off. Here V_{gs} is 0 volt. In case of depletion type MOSFETS we can either increase or decrease the value of V_{gs}. if we make it -0.5 volt or +0.5v In case of V_{gs} +0.5 the gate terminal become positive and if the gate terminal becomes positive and attract more electrons, as the number of electrons increases the current will also increases, so for V_{gs} the drain current I_D will be larger when V_{gs} is positive.

(b) Sketch the hybrid model and write equations for the transistor in common emitter configuration.

Solution:





In common emitter transistor configuration, the input signal is applied between the base and emitter terminals of the transistor and output appears between the collector and emitter terminal. The input voltage (V_{be}) and the output current (i_e) are given by the following equations:

$$V_{be} = h_{ie} \cdot i_b + h_{re} \cdot V_c$$

$$i_e = h_{fe} \cdot i_b + h_{oe} \cdot V_c$$

⇒ Transistor hybrid Model CE Configuration:-

where

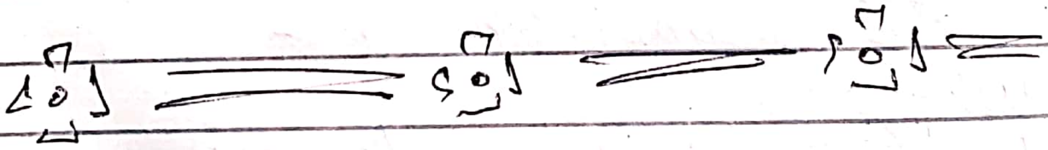
$$h_{ie} = (\partial f_1/\partial i_B)V_c = (\partial v_B/\partial i_B)V_c = (\Delta V_B/\Delta i_B)V_c = (V_b/i_b)V_c$$

$$h_{re} = (\partial f_1/\partial v_c)\, I_B = (\partial v_B/\partial v_c)\, I_B$$
$$= (\Delta v_B/\Delta v_c)\, I_B = (v_b/v_c)\, I_B .$$

$$h_{fe} = (\partial f_2/\partial i_B)\, v_c = (\partial i_c/\partial i_B)\, v_c$$
$$= (\Delta i_c/\Delta i_B)\, v_c = (i_c/i_b)\, v_c$$

$$h_{oe} = (\partial f_2/\partial v_c)\, I_B = (\partial i_c/\partial v_c)\, I_B$$
$$= (\Delta i_c/\Delta v_c)\, I_B = (i_c/v_c)\, I_B$$

The Same theory is extended to other configurations including CB and CC.



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