(1)

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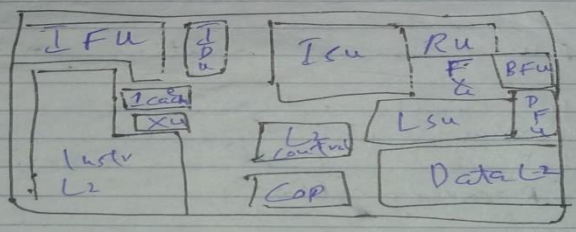
Q No 1 Give answer to each of the following.

(A) Draw the IBM Z Enterprise EC12 core layout and explain the function of each sub-area.



IDU (instruction decode unit):-

The IDU is responsible for the parsing and decoding of all Z/Architecture operation codes.

LSU (Load Store Unit) :-
It is responsible for handling all type of operand access of all lengths, modes and formats.

XU (Translation Unit) :- This unit translate logical address from instruction into physical addresses in the main memory.

FXU (Fixed point unit) :- The FXU executes fixed point arithmetic operations.

BFU (binary floating point unit) :- The BFU handles all binary and hexadecimal floating point operations.

DFU (Decimal floating point unit) :- The DFU handles both fixed point and floating point operations on numbers that are stored as decimal digits

RU (Recovery Unit) :- The RU keeps a copy of complete state of the system that include all registers.

COP (Dedicated co-processor) :- The COP is responsible for data compression and

encryption function for each core

I - cache :- This is a 64 kb LI instruction cache allowing the IFu to prefetch instruction before they are needed.

L2 cache :- This is the control logic that manages the traffic through the two L2 cache

Data L2 :- 1 Mb L2 cache for all memory traffic other then instruction.

Instr L2 :- 1 Mb instruction cache

(B) Discuss the IAS operation in detail.

Ans The IAS operates by respectively performing on instruction cycle consists of two sub cycles.

(a) Fetch cycle :- The control circuitry cycle interrupts the opcode and executes the instruction. by sending out the appropriate control signal to cause data to be moved or an operation to be performed by ALU. And this instruction perhaps taken from the IBR.

(b) Execute Cycle :- The control circuitry interrupts the opcode & execute the

the instruction by sending out the appropriate control signal to cause data to be moved or an operation to be performed by the ALU.

(C) What is embedded system? list different embedded system used in everyday life?

Ans Often embedded system are tightly coupled to their environment. This can give rise to real time constraints such as required speed of motion, This imposes more comple real time constraints list of everyday life:-
Such as Cellphone, digital cameras, Video cameras, calculators, Microwave Washing machines etc.

(D) Discuss different desktop applications that require the great power of Contemporary microprocessor - based - system?.

Ans The given below are the application that require the great power of contemporary based Microprocessor - system
(1) Image processing (2) three dimensional rendering (3) Speech recognition (4) Video conferencing (5) Simulation Modelling

(E) Discuss the techniques used in contemporary processor to increase speed?

Ans Here some of the techniques used to increase the speed are
(1) Piplining:- Piplining enable to processor to work simultaneously on multiple

instructions by performing a different phase for each of the multiple instruction

(2) Branch prediction :- Branch predition potentially increase the amount of work available for the processor to execute.

(3) Superscaler Execution :- This is the ability to issue more then on instruction in every processor clock cycle.

(F) Discuss the problems created due to increase in clock speed in logic density of the processor?

Ans The problem which is created due to increase the clock speed and Logic density of the processor are given below:

Power :- As the density of logic and the clock speed on a chip are increased so the power density increases and also dissipated that heat.

Memory latency :- Memory access speed (latency) and transfer speed (through put) of processor speed.

(G) Discuss the speed up of a program using multiple processors compared to a single processor using Amdahls law.

Ans The speedup using a parallel processor with N processors that fully exploits the parallel position of the program is as follo

Speedup = time to execute program on a single processor / time to execute program on N parallel processor

$= T(1-f) + Tf / T(1-f) + Tf/N =$

$= 1/(1-f)$

(II) Discuss the multicore, Mic and GPGPU in detail?

Multicore :- The use of multicore processor on the same chip provides the potential to increase performance without increasing the clock ratio.

MIC :- Leap in performance as well as the challenges in developing software to exploit such a large number of core.

GPGPU :- Core designed to perform parallel operations on graphic data. it is used to encode and render 2D and 3D graphics.

(I) Discuss the quickpath Interconnect (QPI) protocol layers.

QPI layers :- In This layer the packet is defined as the unit of transfer. One key function performed at this level is a cache coherency protocol, which deals with making sure that main memory values held in multiple cache are consistent. A typical

data packets payload is a block of data being send to or from a cache.

(J) Discuss the physical and logical Architecture of PCIe in detail.

Ans A root complex device also refferred to as a chipset or a host bridge connects the processor and memory sub system to the PCI express switch fabric comprising one or more PCIe and PCIe switch device.
PCIe links from the chipset may attached to a following devices.

(1) Switch :- The switch manages multiple PCIe streams.

(2) PCIe end point :- An I/O device or controller that implement PCIe such as Gigabit ethernet switch disk interface or communication controller etc.

(3) PCIe or PCI bridge :- Allows older PCI devices to be connected to PCIe based system.

Q No. 2

(A) Main structural components of a Computer?

Ans Main four components of a computer

CPU CPU controls the operation of the computer and perform data processing.

Main Memory :- In which we store data.

System Interconnection :- some mechanism that provides for the communication.

I/O :- It moves data from computer to external device and vise versa.

(B) Key characteristics of a planned computer family?

Similar or identical Instruction Set :- This mean that program can move up but not down.

Identical operating system :- The same basic OS is available for all family members.

Increasing Number of I/O parts :- The number of I/O parts increases in going from lower to higher family.

Increasing Memory sizes :- Increasing the Main memory size is going to family

Increasing costs :- Increasing costs its going from lower to higher family member.

(C) Stored program Computer :- The first generation computers used vacuum tubes for digital logic elements. A fundamental design approach first implemented in the IAS computer is known as the stored program concept and Now a

day main memory which stored both data and information.

(D) Moor's law :-

Ans Gordon Moore observed that the number of transistors was doubling every year on a single chip the pace slowed to doubling every 18 mth. in the 1970's but has substained that ratio since.

(1) The cost of computer
(2) the electrical path length is shortened increasing operating.
(3) The computer becomes smaller.

(E) Instruction cycle state diagram :-

Ans Instruction fetch :- Read instruction from its memory location into the processor.

Instruction operation decoding (iod) :- Analyze instruction to determine type of operation to be performed and operand(s) to be used.

Operand address calculation (oac) :- If the operation involves reference to an operand in memory or available via I/O Then determine the address of the operand.

Operand fetch :- Fetch the operand from memory or read it in form I/O.

Data operation :- Perform the operation indicated in the instruction

Operand store :- Write the result into memory or out to I/O.

(F) Classes of interrupts?

Ans Classes of Interrupts :-

Program :- Its generated by some condition that occurs as a result of an instruction execution such as arithmatic overflow dimension by zero or reference outside a user allowed memory spaces

Hardware failure :- It is generated by a failure such as power failure or memory parity failure - error.

Timer :- It is generated by a timer within the processor. This allow the operating system to perform certain functions on a regular basis.

I/O :- It is generated by an I/O controller to single normal completion of an operation request service from the processor.

(G) Bus Interconnection scheme?

Ans The most common computer interconnection structures are based on the use

of on or more system buses.
A system has consists typically of from about fifty to hundered lines There are given below:

Data line :- Data line provide path for data to move of among system module.
Address line :- It catches the addresses of data that move from one to another.
Control line :- And this lines control the above line I to write, transfer ALK.

Q No 3 Differentiate each of the following.

(A) Computer Organization and Computer architecture

Ans: Computer Architecture :- Refers to those attributes of a system visible to a programmer or, put another way those attributes that have a direct impact on the logical execution of program.
Computer organization :- Refers to the operational units and their interconnection that realyze the architecture specifications.
Example Architecture attributes include the instruction set e.g. numbers characters or I/o mechanisms.

(B) RISC and CISC

Ans RISC :- Reduced instruction set computers. The ARM architecture is used in a wide variety of embedded system and is one of the most powerful and best designed RISC based system on the market.

CISC :- The x86 incorporates the sophisticated designed principles once, found only on main frames and super computers and serves as an excellent example of CISC design.

(C) Microprocessors and Microcontroller?

Microprocessor :- Chip included register an ALU and some sort of controls unit or instruction processing logic. A transistor density increase it become possible to increase the complexity of the instruction set architecture and ultimately to add memory and more then one processor.

Microcontroller :- Chip makes a substaintially different use of the logic space available, a microcontroller is a single chip that contains the processor, non-volatile memory for the program (ROM).

(D) Cortex – A, Cortex – R and Cortex – M?

Ans Cortex – A :- The cortex A and cortex A-50 are application processor intendent for mobile devices such as smartphones and E-book readers, digital tv, home gate way etc.

Cortex – R :- The cortex – R is designed to support real – time application in which the timing of event need to be controlled with rapid response to events. They run at a high frequency e.g 200 MHz to 800 MHz.

Cortex – M :- Cortex – M series processors have been developed primary for the microcontroller domain where the need for fast highly deterministic interrupt management is coupled with the desire for extremely low gate count and lowest possible power consumption

(E) Program flow of control without interrupt and with interrupt.

Ans → In the interrupt cycle, the processor cheaks to see if any interrupts have occured, indicated by the presense of an interrupts signals.

→ If no interrupt are pending, the processor proceeds to the fetch cycle and fitches the

the next instruction of the current program.

(F) Disabled interrupt and nested Disabled interrupt processing?

Ans Disabled interrupt:- Simply mean that the processor can and will ignore that interrupt request signal.

Nested interrupt:- Is to allow an interrupt of higher priority to cause a lower priority interrupt handler to be itself interrupted.

(G) Programing in hardware and programing in software?

Programing in hardware:- Suppose we construct a general purpose configuration of arithmatic and logic functions. This set of hardware perform remains functions on data in the original case of customized hardware, the system accepts data and produced results

Programing in software:- The new method programing in much easier. instead of rewriting the hardware for each new program, all we need to do is provide a new sequence of code, each code is in effect, an instruction and part of the hardware interrupts each instruction and generates control signals.

Q No 4

(D)

Ans

(a) Since we have the same instruction mix, that means the additional instruction for each task could be allocated appropriately between the instruction types. Therefore, the following table be gotten:

Instruction type	CPI	Instruction mix
→ Arithmetic And Logic	1	60%
→ Load / store with cache hit	2	18%
→ Branch	4	12%
→ Memory reference with cache miss	12	10%

Average CPI = $(1 \times 0.6) + (2 \times 0.18) + (12 \times 0.12) + (12 \times 0.1) = 2.64$

Therefor the CPI has been increased since the time for memory access is also increased.

(b) Mips rate = $400 / 2.64 = 152$

Therefore, the corresponding drop in the Mips rate

(c) $T = Ic / (Mips \times 10^6)$

For one processor $T_1 = (2 \times 10^6) / (178 \times 10^6) = 11$ ms

For 8 processors

$$T_8 = \frac{\frac{2 \times 10^6}{8} + 0.025 \times 10^6}{2 \times 10^6} = 1.8 \text{ ms}$$

$$\text{Speed up} = \frac{\text{time to execute program on single processor}}{\text{" N parallel processor}}$$

$$= \frac{11}{1.8} = 6.11$$

(d) Infact, there are two inefficient in the parallel system
The first one is that there are more additional instruction which is added to coordinate between threads.
The second one is that there is contention for memory access. Thus, none of the code is inherntly serial and all of its parallelizable but with scheduling overhead.
By depending on the information given, it is not obvious how to quantify this effect on the Amadahls law
Therefore, supposed that the fraction of code, which is parallelizable, is $f = 1$ then Amadahl's law decreases to speedup $= N = 8$, Therefore the actual speedup is only about 73% of the theoratical speedup.

Q No 4 (g)

Ans

Since the clocking rate 4 MHz, the bus cycle will need 0.25 μs. Thus, the memory cycle will take $0.25 \times 4 = 1$ μs.
By applying this if an odd-aligned word is referenced, two memory cycles, each consisting of four bus cycles, are required to transfer the word, from the question, so we will have three cases:
First is if both operands are even-aligned so the time required is $1 \times 2 = 2$ μs to fetch both operands.
Second case is if both operands are odd, so the allowed required is $1 \times 4 = 4$ μs to fetch the operands.
Third case is if only one is odd-aligned, so the time required is $1 \times 3 = 3$ μs to fetch both operands.

(F)

Ans

(a) $2^{(32-8)} = 2^{24} = 16,777,216$ byte
$= 16$ MB, (8 MB = 1 byte for opcode)

(b)
(1) 32 bit local address bus and a 16 bit local data bus. Instruction and data transfer would take three bus cycles each, one for the address and

two for the data. Since if the address bus is 32 bits, the whole address can be transfered to memory at once and decoded there; however, since the data bus is only 16 bits, it will require 2 bus cycles (accesses to memory) to fetch the 32 bit instruction or operand

(2) a 16 bit local address bus and a 16 bits local data bus, instruction and data transfer would take four bus cycles each, two for the address and two for the data. Therefore, that will have the processor perform two transmissions in order to send to memory the whole 32 bit address; this will require more complex memory interface control to latch the two halves of the address before it perform an access to it.

(C) For the PC needs 24 bits (24 bit address) and for the IR needs 32 bits (32 bit addresses)

Q No 4 (C)

Effective CPI

$CPI = (1 \times 46000) + (2 \times 33000) + (2 \times 16000) + (2 \times 9000) / 100$

$CPI = 162000 / 100$

$CPI = 1620.$

Mips rate = 60 M+g / 1620 × 10^6

Mips rate = 60 × 10^6 / 1620 × 10^6

Mips rate = 60 / 1620

Mips rate = 0.037

Execution time

T = Ic / (Mips × 10^6)

T = 104000 / (0.037 × 10^6)

T = 104000 / (37 × 10^3)

T = 2811 × 10^3

T = 2.811 second

Q 4 (B)

Ans

Following two memory addresses

Opcode	operand
00000001	0000000000001

In the beginning, the CPU have to fetch the instruction from the memory. Then the instruction will include the address of the data which is required to load. through the execution the memory will be accessed in that time to load data contents which is located at that for a total of two trips to memory.

Q No 4 (A)

(a) Following Assembly language code for given addresses.

Address	Contents
08A	Load M (0FA)
	Store M (0FB)
08B	Load M (0FA)
	Jump +M (08D)
08C	Load -M (0FA)
	Store M (0FB)
08D.	

(b) This program is to store the absolute value of content at memory location 0FA into memory 0FB.