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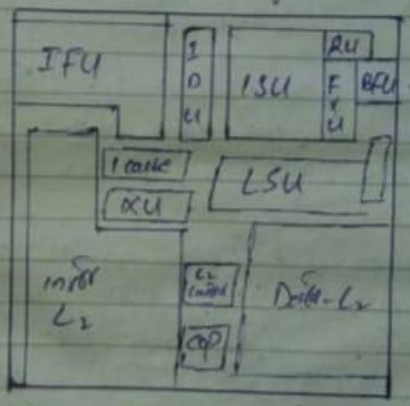
Computer Architecture

Q1 Give answer to each of the following?

Ans (A)



* IDU ☞ stand for instruction decode unit
The IDU is responsible for the parsing and decoding of all z/Architecture operation codes.

* LSU ☞ stand for load store unit.
It is responsible for handling all type of operand access of all length modes and formats.

* XCU ☞ stand for Translation unit
This unit translate logical address from instruction into physical address in the main memory.

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* FXU :- The FXU executes fixed point arithmetic operation.

* BFU :- stand for Binary floating point unit The BFU handles all binary and hexadecimal floating point operations.

* DFU :- stand for Decimal floating point unit The DFU handle both fixed point and floating point operation on number that are stored as decimal digits.

* RU :- (Recovery unit) The RU keeps a copy of the complete state of the system that include all register.

* COP :- (Dedicated co-processor) The COP is responsible for data compression and encryption function for each core.

* I-cache :- This a 64 kb L1 instruction cache memory allowing. The IFU to prefetch instruction before they are needed.

* L2-caches :- This is control logic that manages the traffic through the two L2-caches

* Data L2 :- 1MB L2 cache for all memory traffic other than instruction.

* Instr L2 :- 1MB instruction cache.

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Ans 'B'

The IAS operates by respectively performing an instruction cycle. Each instruction cycle consists of two sub-cycle.

1) Fetch cycle :- The opcode of next instruction is loaded into the IR and the address portion is loaded into the MAR. This instruction perhaps taken from the IBR.

2) Execute cycle :- The control circuitry interprets the opcode & executes the instruction by sending out the appropriate control & signal to cause data to be moved or an operation to be performed by the ALU.

Ans 'C'

Often embedded system are tightly coupled to their environment. This can give rise to real time constraint such as required speed of motion this imposes more complex real time constraints out of daily life.
Such as cellphone video camera, home security system washing machines digital camera traffic system.

Ans 'D'

The given below are the application that require the great power of contemporary microprocessor system are 1) image processing 2) Three dimension 3) speech recognizing 4) video conferencing 5) Multimedia Authoring 6) voice and video annotation of files 7) simulation modelling

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Ans'E,

Here some of techniques used to increase the speed are

1) pipelining or pipelining enable to processor to work simultaneously on multiple instruction by performing a different phase for each of the multiple instruction ~~by p~~

2) Branch prediction or Branch prediction potentially increase the amount of work available for the processor to execute.

3) Superscalar execution or This is the ability to issue more than one instruction in every processor clock cycle.

4) Data flow analysis or The processor analysis which instruction are dependent on each other results or data to create an optimized schedule of instruction.

5) speculative execution or This enables the processor to keep its execution engines as busy as possible by executing instruction that are likely to be needed.

Ans'F,

The problems which is created due to increase the clock speed and logic density of the processor are given below.

Reasons or As the density of logic and the clock speed on a chip increase so the power density increase and also dissipated that heat.

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Redelay ⇒ The speed at which electrons can flow on a chip b/w transistors is limited by the resistance and capacity of the metal wires connecting the specifically delay increase as the the prochet increase.

Memory latency ⇒ Memory access speed (latency) and transfer speed (Throughput) Any Processor speed

Ans 4, The speedup using a parallel processor with N processor that fully exploits the parallel portion of the program is as follow.
speedup time to executes program on a single processor / time to execute program on N parallel processor =

$$T(1-f) + Tf / T(1-f) + Tf/N =$$
$$1/(1-f) + f/N .$$

Ans 5, Multicore ⇒ The use of Multiplore Processor on the same chip provides the potential to increase performance without increasing the clock rate.

MIC ⇒ leap in performance as well as the challenges in developing software to exploit such a large number of core

GPGU ⇒ core designed to perform parallel operations on graphic data it is used to encode and render 2D and 3D Graphics as well as processor video.

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Ans 4, QPI protocol layer or
In this layer, the packet is defined as the unit of transfer. One key function performed at this level in a cache coherency protocol, which deals with making sure that main memory values held in multiple caches are consistent. A typical data packet payload is a block of data being sent to or from a cache.

Ans 5. Physical and logical Architecture of PCIe

* A root complex device also referred to as a chipset or a host bridge connects the processor and memory subsystem to the PCI Express switch fabric comprising one or more PCIe and PCIe switch devices.
* PCIe links from the chipset may attach to the following kind of devices that implement PCIe.
* Switch : The switch manages multiple PCIe streams.
* PCIe endpoint : An I/O device or controller that implements PCIe such as Gigabit ethernet switch a graphics or video controller disk interface or a communications controller.
* Legacy endpoint or legacy endpoint category is created for existing designs that have been migrated to PCI Express and it allows legacy behaviors such as use of I/O space and locked transactions.
* PCIe/PCI bridge : Allows older PCI devices to be connected to PCIe-based systems.

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Q2

Ans a)

Main structural components of a computer.
There are four main structural components.

1) CPU or controls the operation of computer and performs its data processing functions; often simply referred to as processor.
2) Main memory or stores data
3) I/O : Moves data b/w the computer and external environment.
4) System interconnection or some mechanism that provides for communication among CPU, main memory and I/O.

Ans b)

The characteristic of a family are as follow

* Similar or identical instruction set or In some cases the lower end of family has an instruction set that is a subset of that of the top end of the family. This means that program can move up but not down.
* Similar or identical operating system or The same basic operating system is available for all family members.
* Increasing speed or The rate of instruction execution increase in going from lower to higher family members.
* Increasing I/O ports or The number of I/O ports increases in going from lower to higher family member.
* Increasing memory size or The size of memory increases in going lower to higher family member.
* Increasing cost or At a given point time, cost of a system increases in going lower to higher family member.

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Ans'c

Stored Program Computer.

A fundamental design approach first implemented in the IAS computer is known as the stored program concept. This idea is usually attributed to the mathematician John von Neumann. The first publication of the idea was in 1945 proposal by von Neiman for a new computer the EDVAC in 1946, von Neumann and his colleagues began the design of a new stored program computer, referred to as the IAS computer at the Princeton institute for Advanced studies.

-- A main memory which stores both data and instructs
-- An arithmetic and logical unit (ALU) capable of operating on binary data.

Ans'd

Moore's Law.

The famous Moore's law which was proposed by Gordon Moore cofounder of intel in 1965 [MOOR65]. Moore observed that the number of transistor that could be put on a single chip was doubling every year. The pace slowed to a doubling every 18 months in the 1970s but has sustained that rate ever since.

Moores law are profund.

1) The cost of computer logic and memory circuitry has fallen at a dramatic rate.
2) Because logic and memory elements are placed closer together on more densely packed chips the electrical path length is shorted increasing operating.
3) The computer becomes smaller making it more convenient to place in a variety
4) There is a reduction in power requirement.
5) with more circuitry on each chip, there are fewer interchip connections.

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Ans 8 E, Instruction cycle state diagram.

The state in instruction cycle can be described as follows.

* Instruction address calculation (IAC): Determine the address of the next instruction to be executed. usually this involves adding a fixed number to the address of the previous instruction.
* Instruction fetch (IF): Read instruction from its memory location into the processor.
* Instruction operation decoding (IOD): Analyse instruction to determine type of operation to be performed and operand(s) to be used.
* Operand Fetch (OF): Fetch the operand from memory or read it in from I/O.
* Data operation (DO): Perform the operation indicated in the instruction.
* Operand Store (OS): Write the result into memory or out to I/O.

Ans 8 F, Classes of interrupts:

I) Program: It is generated by some condition that occurs as a result of an instruction execution such as arithmetic overflow, division by zero, attempt to execute an illegal machine instruction, or reference outside a user's allowed memory space.

II) Timer: It is generated by a timer within the processor. This allow the operating system to perform certain function on a regular basis.

III) I/O: It is generated by I/O controller to signal normal completion of an operation, request service from the processor or to signal various error conditions.

IV) Hardware failure: It is generated by failure such as power failure or memory parity error.

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Ans 'C,

Bus interconnection scheme

The most common computer interconnection structure, are based on the use of one or more system buses.

(a) Data lines :- The data lines provide a path for moving data among system modules. These lines collectively are called the data bus.

(b) Address lines :- The address line are used to designate the source or destination of the data on the data bus. The width of address bus determines the maximum possible memory capacity of the system.

(c) Control lines :- The control line are used to control the access to and use of data and address lines Because the data and address lines, are shared by all components. Typical control lines include: Memory write, Memory read, I/O write, I/O read Transfer-ACK, Bus request, Bus grant, interrupt request, interrupt ACK, clock and Reset.

Ans 'B,

Ans 'A,

Computer organization and Architecture:

* Computer Architecture refer to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program. A term that is often used interchangeable with computer architecture is instruction set architecture (ISA).

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* Computer organization ⇒ Refer to the operational units and their interconnection that realize the architectural specification. Examples of architectural attributes include the instruction set, the no. of bits used to represent various data types (e.g., number, characters), I/O mechanism and techniques for addressing memory.

Ans B)

RISC and CISC

* The current x86 offering represents the result of decade of design effort on complex instruction set computer (CISC). The x86 incorporates sophisticated design principles once found only on mainframes and supercomputer and serves as an excellent example of CISC design.

* An alternative approach to processor design is the reduced instruction set computer (RISC). The ARM architecture is used in a wide variety of embedded system and is one of the most powerful and best designed RISC-based system on the market. In the section and the next we provide a brief overview of these two systems.

Ans C)

Micro Processor ⇒ Chip included register an ALU and some sort of control unit or instruction processing logic. A transistor density increased it become possible to increase the complexity of the instruction set architecture and ultimately to add Memory.

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and more than one processor.

Micro controller :- chip makes a substantially different use of the code space available. a micro controller is a single chip that contains the processor non-volatile memory for the program (ROM)

Ans 5) D)

cortex A :- The cortex A and cortex A50 are application processor intended for mobile devices such as smart phones and Ebook readers digital tv. home gate way etc.

cortex R :- The cortex R is designed to support real time application in which the timing of events need to be controlled with rapid response to events they run at higher frequency eg (200 MHz to 800 MHz)

cortex M :- cortex M small processor have been developed primary for the micro controller domain while the need for fast highly deterministic interrupt management is coupled with the desire for extremely low gate count and lowest possible consumptions.

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Ans 5 E,

Program flow of control without interrupt and with interrupt -

1) In the interrupt cycle the processor checks to see if any interrupt have occurred indicated by the presence of an interrupt signals.

2) if no interrupt are pending the processor proceeds to the fetch and fetches the next instruction of the current program.

Ans 5 F,

Disabled interrupt and masked interrupt

Disabled interrupt is simply mean that the processor can and will ignore that interrupt request signal.

Masked interrupt is to allow an interrupt of higher priority to cause a lower priority interrupt handler to be it self interrupted.

Ans 5 G,

Programing in Hardware is suppose we construct a general purpose configuration of arithmatic and logic functions. This set of hardware will perform various function on data in the original case of customized hardware the system accept data and produced result.

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Programing in Software

The new method programing is much easier instead of rewriting the hardware for each new program. All we need to do is provide a new sequence of code. Each code is in effect an instruction and part of the hardware interrupt each instruction and generates control signal.

Q4/5

Ans 'A' 3) 1) Here is a simple way to understand this problem.

content are divided up into two shift instruction LH and RH

LH instruction = 010FA

opcode = 01

address = 0FA

RH instruction = 210FB

opcode = 21

address = 0FB

since this in hexadecimal form you have to convert this number to binary form.

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LH instruction is 01 = 00000001 = LOAD M(x)
Refer to the memory address location 0FA
The first shift of 08A should read - LOAD M(0FA)

RH instruction is
2A = 00100001 = STOR M(x)
M(x) refer to the memory address location 0FB

The second shift of 08A should read - STOR M(0FB). Finally the assembly language for 08A 0|0FA|0FB

(0AA) M(0FA)
STOR M(0FB)

2) Here is a simple way to understand this problems.
Contents are divided up into two shift instruction LH and RH.

LH instruction = 0|0FA
opcode = 01
address = 0FA
RH instruction = 0F08D
opcode = 0F
address = 08D

Now convert this number into Binary form.

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LH instruction eg

01 = 00000001 = LOAD M(x)

M(x) refer to memory address location FA

The first 8bits of 0x8 should read = LOAD M(0FA)

RH instruction eg 0F = 00001111 = JUMP+M(x,

refer to memory address location 0x0

The second 8bits of 0x8 should read = JUMP + M(0x0, 0:19)

Finally the assembly language codes for 0x8 0x0FA0F0x0 is -

LOAD M(0FA)

JUMP+M(0x0, 0:19)

3) Here is a simple way to understand this problem.

contents are divided into two 8bits instructions.

LH instruction = 020FA

opcode = 02

address 0FA

RH instruction = 210FB

opcode = 21

address = 0FB

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Since this is hexadecimal form, you have to convert the number to binary form.

LM instruction as

02 = 00000010 = LOAD - M(x)

M(x) refer to memory address location OFA

The first shift of 08 should read LOAD - M(OFA)

RM instruction as 21 = 00100001 = STOR M(x)

M(x) refer to memory address location OFB

The second shift of 08 should read - STOR M(OFB)

Finally the assembly language code for 08C 020FA210FB is

LOAD - M(OFA)
STOR M(OFB)

Ans b

1) In 08A address the M(OFA) Transfer to the accumulator and transfer contents of accumulator to memory location OFB.
2) In 08B address the M(OFA) Transfer to the accumulate and take next instruction from left half of M(08D)

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3) In 08C address the -M(OFA) Transfer to the accumulate and transfer content of accumulate to memory location.

Ans c/s

Effective CPI =

$$CPI = (1*46000)+(2*33000)+(2*16000)+(2*9000)/100$$

$$CPI = 162000/100$$

$$CPI = 1620$$

MIPS Rate =

$$= 60 MHz / 1620 * 10^6$$

$$= 60 \times 10^6 Hz / 1620 * 10^6$$

$$= \frac{60 Hz}{1620}$$

MIPS Rate = 0.037

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Execution Time is

$$T = Ic / (MIPS * 10^6)$$

$$T = 104000 / (0.037 * 10^6)$$

$$T = 104000 / 37 * 10^3$$

$$T = 2811 \times 10^{-3}$$

$$T = 2.811 \text{ sec}$$

Ans 5 D,

Since we have the same instruction mix that means the additional instruction for each task could be allocated appropriately between the instruction type Therefore the following table be gotten

Instruction Type	CPI	Instruction Mix
Architecture and logic	1	60 %
Load/Store with cache hit	2	18 %
Branch	4	12 %
Memory reference with cache miss	12	10 %

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The average CPI = (1×0.6) + (2×0.18) + (4×0.12) + (12×0.1)

CPI = 2.64

Therefore CPI has been increased since the time for memory access is also increased.

b) MIPS = 400/2.64 = 152

There is a corresponding drop in the MIPS rate

c) The speedup factor equal to the ratio of the execution times.

The execution time is calculated as the following

$T = I_c / (MIPS \times 10^6)$

For one process $T_1 = (2*10^6) / (171*10^6)$

T_1 = 11ms

For 8 processor each process executed 1/8 of the 2million instruction plus the 25,000

$T_8 = 2*10^6/8 + 0.025$

1.52×10^6

T_8 = 1.8 ms

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speedup = Time to execute program on a single processor / Time to execute program on N parallel processor

speedup = 11/1.8

speedup = 6.11

d) By depending on the information given it is not obvious how to quantify this effect in Amdahl's equation. Therefore if it is supposed that fraction of code which is parallelizable is $f = 1$ then Amdahl's law decrease to speed $N = 2$. Therefore the actual speedup is only about 75% of the theoritical speedup.

Ans 5 e) Six steps

1) (a) The PC contains 300 the address of the first instruction. This value is loaded into the MAR.

(b) The value in location 300 (which is the instruction with the value 1940 in hexadecimal) is loaded into the MBR.

and the PC is interchanged. These two steps can be done in parallel.

(c) The value in the MBR is loaded into the IR.

2) (a) The address position of the IR (940) is loaded into the MAR.

(b) The value in location 940 is loaded into the MBR.

(c) The value in the MBR is loaded into the AC.

3) (a) The value in the PC (301) is loaded into the MAR.

(b) The value in location 301 (which is the instruction with the value (5941)) is loaded into the MBR and the PC is incremented.

(c) The value in the MBR is loaded into the IR.

4) (a) The address position of the IR (941) is loaded into the MAR (b) value in location 941 is loaded in to the MBR.

(c) The value of location MBR are added and the result is stored in the AC.

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5) (a) The value in the PC (302) is loaded into the MAR.
(b) The value in location 302 (which is the instruction with the value 2941) is loaded into the MBR, and the PC is incremented.
(c) The value in the MBR is loaded into the IR.

6) (a) The address portion of the IR (941) is loaded into the MAR.
(b) The value in the AC is loaded the MBR
(c) The value in the MBR is stored in location 941.

Ans 5 (a) $2^{24} = 16$ MBytes

(b) (1) if the local address bus is 32 bit the whole address can be transferred at once and decoded in memory. However because the data bus is only 16 bits, it will require 2 cycles to fetch a 32 bit instruction or operand.

(2) The 16 bits of the address placed on the address bus can't access the whole memory interface control is needed to latch and store both parts of the address and then the second part.

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(c) The program counter must be at least 24 bits. Typically a 32-bit microprocessor will have a 32 bit external address bus and a 32 bit program counter, unless onchip segment register are used that may work with a smaller program counter if the instruction register is to contain the whole instruction, it will have to be 32-bit long if it will contain only the op code (called the op code register) then it will have to be 8bits long.

Ans 5 (c) A bus cycle takes 0.25 μs, so a memory cycle takes 2 μs. It take 2 μs to fetch the two operand. if one is odd aligned the time required is 3 μs. if both are odd aligned, the time required is 4 μs.